Oxidized Silicon-On-Insulator (OxSOI) from Bulk Silicon: a New Photonic Platform

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Abstract

- Demonstrate a bulk silicon alternative to SOI, using Si_3N_4 masking and oxidation techniques
- Waveguide losses of 2.92 dB/cm with a process compatible with the front-end of a typical CMOS fabrication line

The present condition

- **Silicon photonics has been made many times over**
- **Sub-wavelength optical wires fabricated using CMOS materials and techniques**

  ➡ ***Feasible and Economic integration of optics and Electronics***

- **High-bandwidth, low-power interconnects**

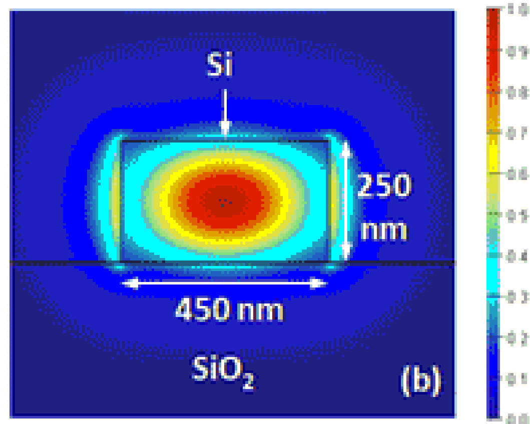
  ➡ ***Can be used for chip multi-processor interconnects or low-jitter chip-wide clock distribution networks***

- **No consensus as to the specifics of how this integration will happen**

" Only that it needs to happen"

Limiting factors of optical material

- **Waveguides**
  - Require a layer of optical cladding
  - Confine it in such a way as to provide directional control of the light
- **High-contrast optics ⇨ reduced the optical wire size**
  - ➢ But typical Si waveguide(450*250nm) requires 1um of SiO_2



- ✓ *SiO2 can be deposited easily*
- ✓ *Cannot be simply inserted beneath*

Limiting factors of optical material

- SOI(Silicon-On-insulator) technology with a large after-process Buried Oxide(BOX) layer
  - BOX layer must be less than a few hundred nanometers to avoid a variety of self-heating effects
  - Would be too small for optical cladding purposes
- One innovative technique
  - Air buffer layer by substrate removal

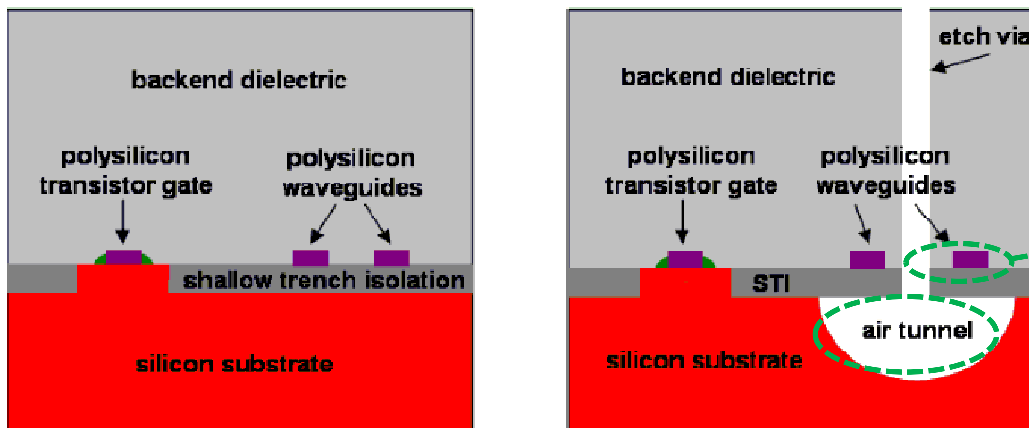
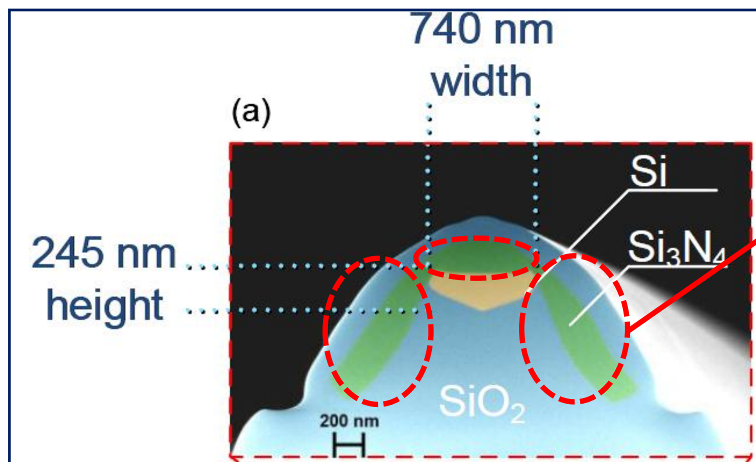


Fig. 1. (left) Sketch of a standard bulk CMOS stack up with fabricated polysilicon waveguides. (right) Sketch after locally removing silicon substrate to eliminate propagation loss due to substrate leakage.

✓ But still used polysilicon as the guiding layer

Goal

- **High quality oxide beneath Si**
  - **Using thermal oxidation ➡ BOX layer**
- **Create waveguide**
  - **By protecting a defined area of bulk silicon**
- **Standard CMOS material and process**
  - **Si3N4 and LOCOS(LOCal Oxidation of Silicon)**



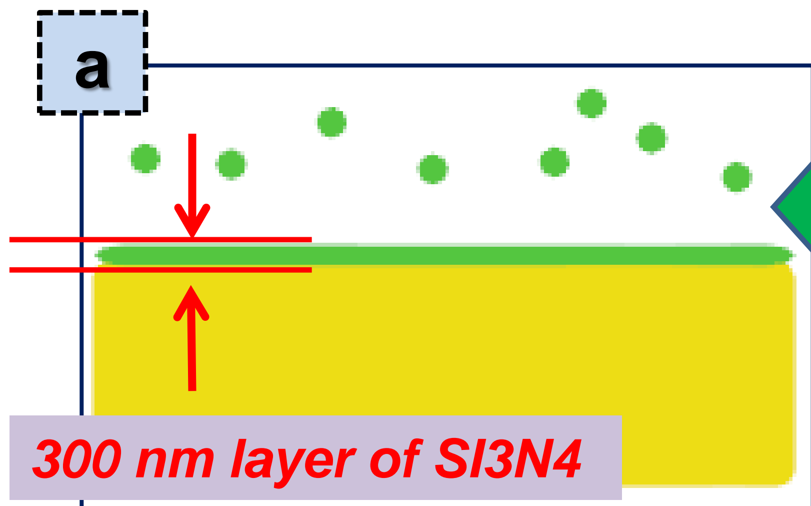
✓ ***Assemble a three sided Si3N4***

➢ ***Fully surrounded channel waveguides on bulk silicon***

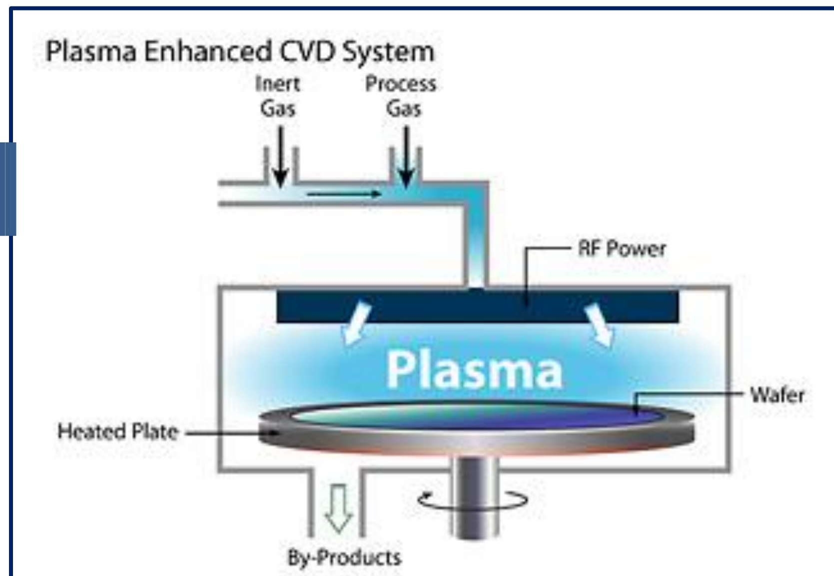
Experimental Work

a. Deposit of Si_3N_4 using PECVD
b. Etching vertically down using ICP etcher
c. Deposit of Si_3N_4 to serve as sidewall
d. Etching the same amount as was deposited
e. Creating BOX layer by oxidation
f. SiO_2 Cladding to complete the surrounding

a. Deposit of Si3N4 using PECVD



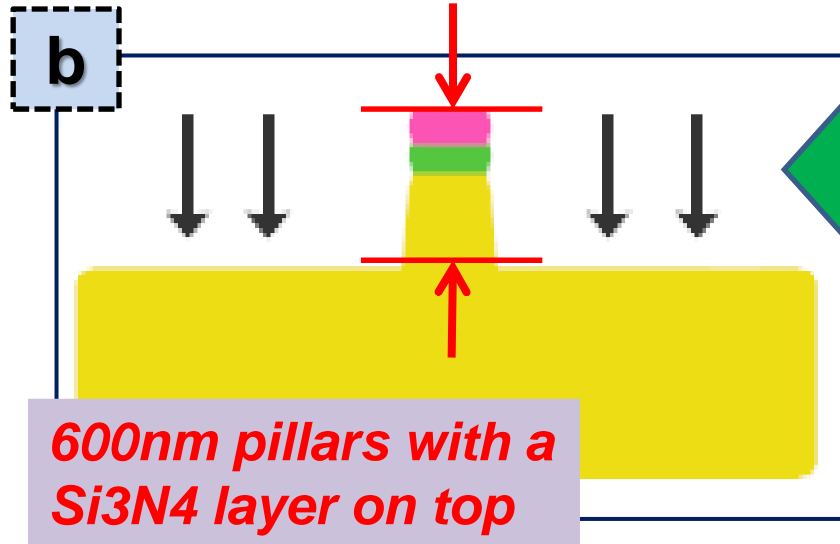
- Silicon
- Si3N4 (first layer)

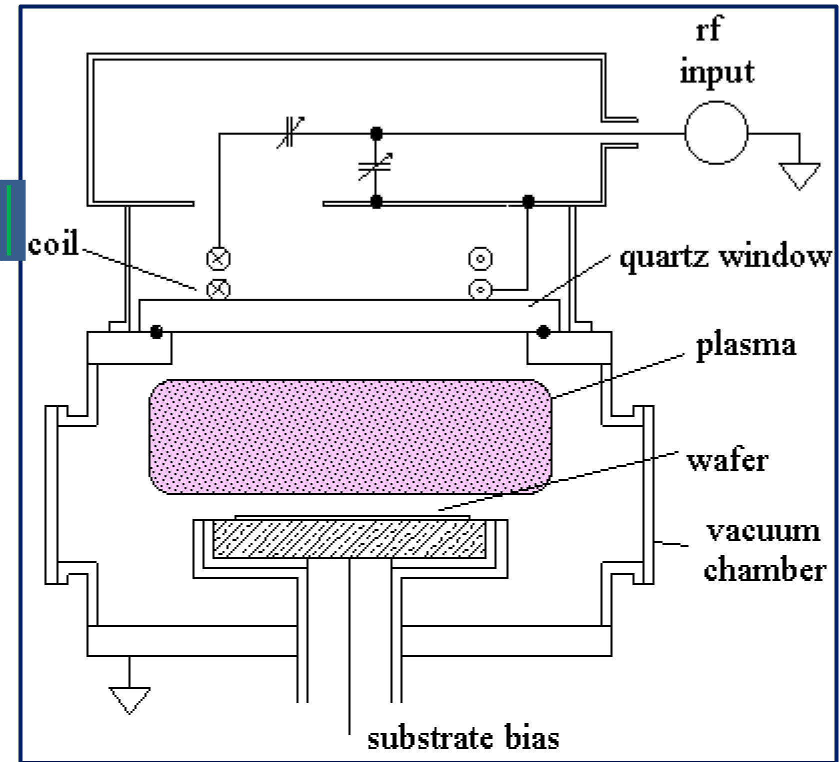


Plasma Enhanced Chemical Vapor Deposition

✓ This layer serves as the top cover the protective mask

b. Etching vertically down using ICP etcher



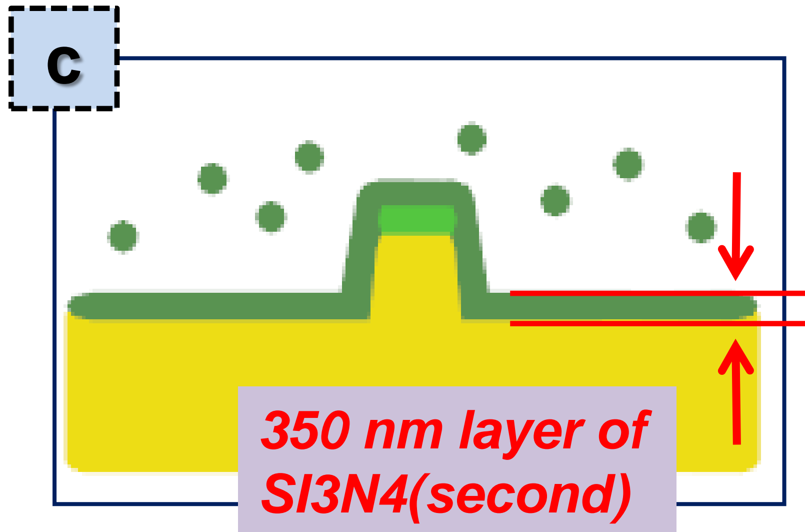


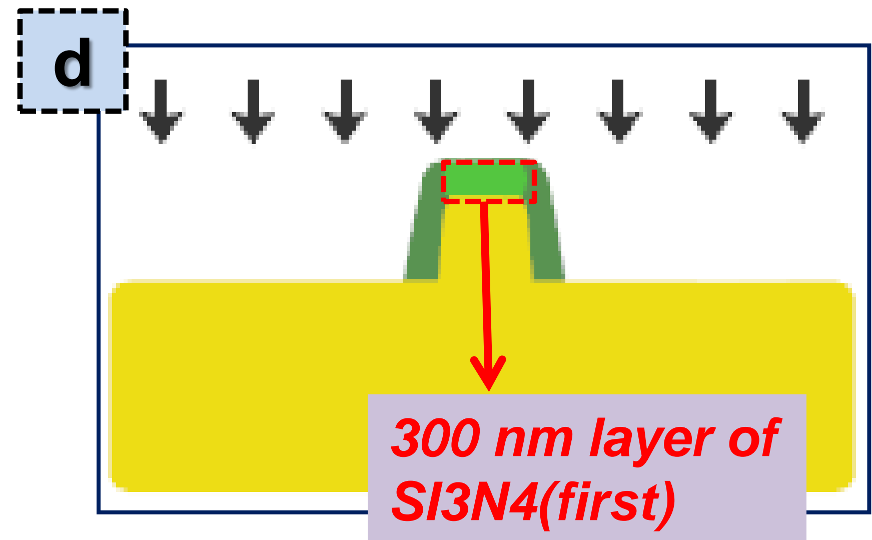
- Silicon
- Si3N4 (first layer)
- Resist

Inductively-Coupled Plasma etching

c. Deposit of Si3N4 to serve as sidewall

d. Etching the same amount as was deposited

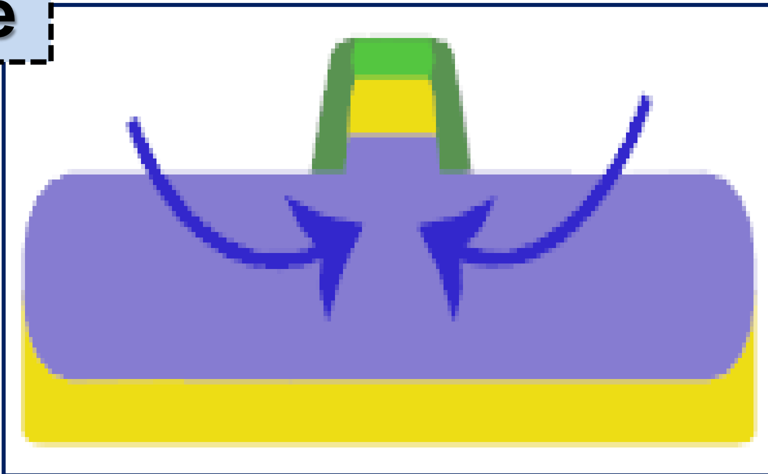


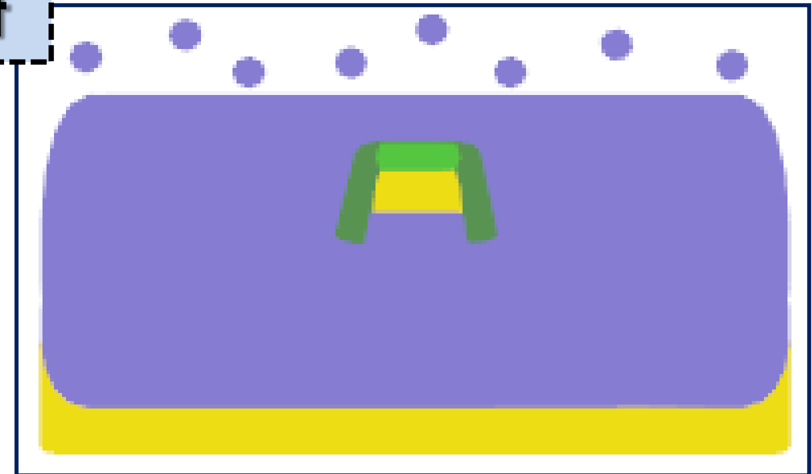


- Silicon
- Si3N4 (first layer)
- Si3N4 (second layer)

e. Creating BOX layer by oxidation

f. SiO2 Cladding to complete the surrounding





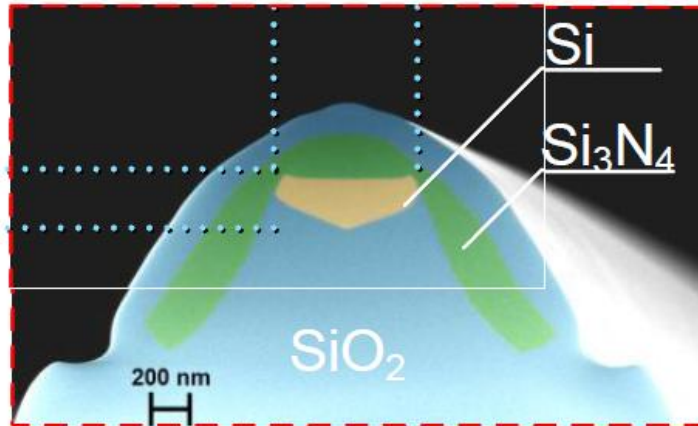
- Silicon
- Si3N4 (first layer)
- Si3N4 (second layer)
- SiO2

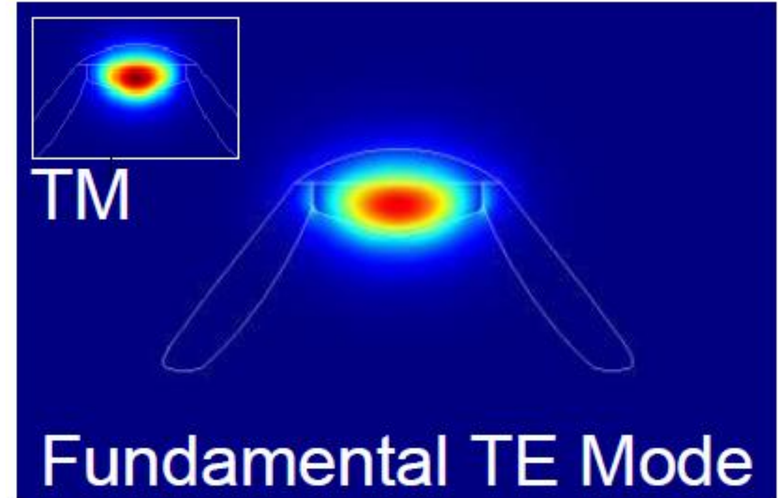
- ✓ **Wet oxidation chamber at 1100°C**
- ✓ **SiO2 grows in the regions of exposed silicon**

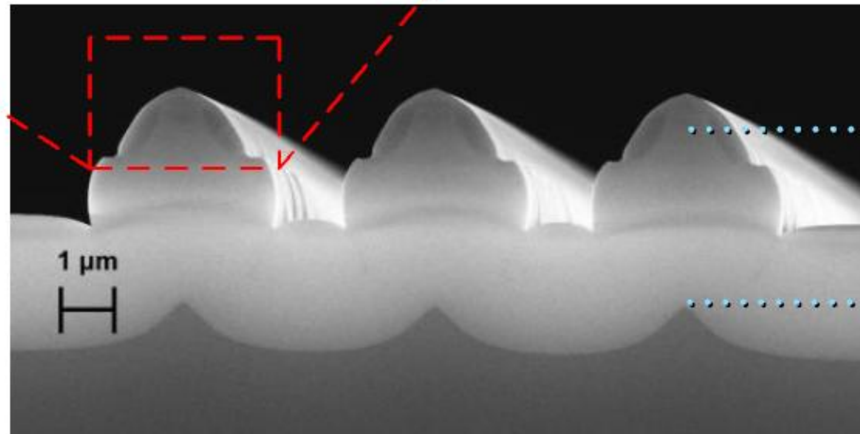
Result & Conclusion

740 nm width

245 nm height

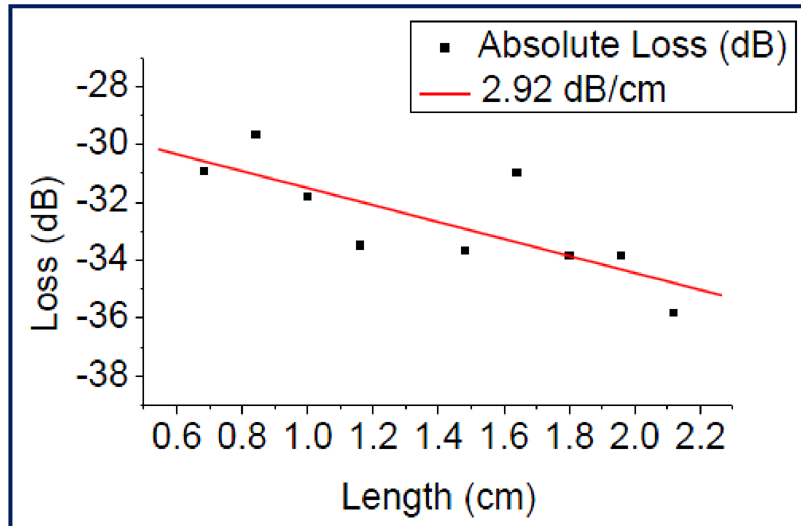






3.3 µm buried oxide

Result & Conclusion



- Propagation loss: 2.92 dB/cm
  - Using the cut-back method
- Similar losses for TE and TM

❖ Confined optical mode

❖ Unaffected by the leftover Si3N4

❖ A sizable BOX layer